

REMARKS/ARGUMENTS

Claims 6 and 11 remain active in the application.

In the outstanding Office Action, claim 6 was rejected under 35 USC 102(b) as being anticipated by U.S. Patent No. 5,286,656 to Keown et al. Claim 11 was objected to as being dependent upon a rejected base claim, but was indicated as being allowable if rewritten in independent format. Applicants respectfully point out that claim 11 was rewritten in independent format in the February 09, 2004 amendment. Applicants acknowledge with appreciation the indication of allowable subject matter.

The official action asserts on page 4 that in Keown et al. gates of the transistors TNMOS and TPMOS are not electrically connected and a gate of one of the transistors TNMOS and TPMOS is connected to a source/drain region of the other transistor via a wire. Applicants admit, in the device shown in figure 2 of Keown et al., the gates of the transistors TNMOS and TPMOS are not electrically connected with each other, and in the device shown in figure 2A a gate of one of the transistors TNMOS and TPMOS is connected to a source/drain region of the other transistor via a wire. However, applicants respectfully point out that Keown et al. state in column 5, lines 56-58 that "alternative configurations for the test pattern transistors TNMOS and TPMOS of FIG. 2 are illustrated in FIG. 2A." Hence, the device shown in figure 2 and the device shown in figure 2A of Keown et al. are distinct devices and that Keown et al. do not teach or suggest that both features are included in a single device. Therefore, it is submitted that the 35 USC 120(b) rejection based on Keown et al. should be withdrawn.

Further, if the feature of the device in figure 2A of Keown et al. were incorporated into the device in figure 2 and a gate of the transistor TNMOS shown in figure 2 were connected to a source of the TPMOS, then the gates of the transistors TNMOS and TPMOS would be electrically connected with each other. Consequently, the device shown in figure 2

at Keown et al. would not anticipate or render obvious one of the features of the present invention, namely, that electrodes of the first and second MOS transistors are electrically insulated from each other. Moreover, the test pads DBP1 and DBP2 of Keown et al. would be electrically connected with each other, causing a disadvantage in that it would become impossible to perform tests for respective transistors TPMOS and TNMOS individually.

Moreover, if the feature of the device in figure 2 were incorporated into the device of figure 2A and the wire connecting the gates of the transistors TPMOS and TNMOS shown in figure 2A were disconnected to electrically insulate the gates of both the transistors, a gate of one of the transistors TPMOS and TNMOS and a source/drain of the transistor would be electrically insulated from each other. Consequently, the device shown in figure 2A of Keown et al. would not anticipate or render obvious one of the features of the present invention, namely, that the gate electrode of the second MOS transistor and the first impurity region of the first MOS transistor are connected via a wire. Moreover, the Vcc voltage would no longer be applied to one of the transistors TPMOS and TNMOS, causing a disadvantage in that it would become impossible to test the transistor.


Further, there is no motivation in Keown et al. to combine the devices shown in figures 2 and 2A. In the device as shown in figure 2 of Keown et al., the gate electrode of one transistor of the CMOS transistors is not connected to a source/drain region of the other transistor. Accordingly, Keown et al. do not disclose or suggest the structural characteristic of claim 6 as described above. Therefore, applicants submit that it is impossible for the device disclosed in Keown et al. to directly observe fluctuation in potential of the gate electrode of said one transistor by using a pn junction in the other transistor.

For the foregoing reasons, the 35 USC 102(b) rejection should be withdrawn. An early and favorable action to that effect is respectfully requested.

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Respectfully submitted,

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